Patent

Docket No.: TRAN-P004.DIV

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	09/15/03	Name of Person Making the Deposit:	ANTHONY CHOU	Signature of the Person Making the Deposit:	Anthony Chou

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Edmund J. Kelly, Robert F. Cmelik and Malcolm J. King

Serial No.: 09/699,947 Group Art Unit:

Filed: 10/30/00 Examiner:

Title: TRANSLATED MEMORY PROTECTION APPARATUS FOR AN ADVANCED MICROPROCESSOR

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

- ____ Formal drawings, totaling ____ sheets.
- ____ Informal drawings, totaling ____ sheets.
- ____ Certification for PTO Consideration
- X Information Disclosure statement (4 sheets)
- ____ Information Disclosure statement and late filing fee
- X Form 1449
- ____ Petition for Extension of Time
- X Other: REFERENCES

F e Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
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[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

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Two North Market Street, Third Floor
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Respectfully submitted,

Date: 15 Sept 2003

By: _____
Matthew J. Blecher
Reg. No. 46,558

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P004.DIV

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Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,349,658	GRAPHICAL USER INTERFACE	09/20/94
5,467,473	OUT OF ORDER INSTRUCTION LOAD AN STORE COMPARISON	11/14/95
5,875,340	OPTIMIZED STORAGE SYSTEM AND METHOD FOR A PROCESSOR THAT EXECUTES INSTRUCTIONS OUT OF ORDER	02/23/99
5,274,815	DYNAMIC INSTRUCTION MODIFYING CONTROLLER AND OPERATION METHOD	12/28/93
6,031,992	COMBINING HARDWARE AND SOFTWARE TO PROVIDE AN IMPROVED MICROPROCESSOR	02/29/00
4,530,050	CENTRAL PROCESSING UNIT FOR EXECUTING INCTRUCTIONS OF VARIABLE LENGTH HAVING END INFORMATION FOR OPERAND SPECIFIERS	07/16/85
5,553,255	DATA PROCESSOR WITH PROGRAMMABLE LEVELS OF SPECULA-TIVE INSTRUCTION FECTCHING AN DMETHOD OF OPERATION	09/03/96
4,896,257	COMPUTER SYSTEM HAVING VIRTUAL MEMORY CONFIGURATION WITH SECOND COMPUTER FOR VIRTUAL ADDRESSING WITH TRANSLATION ERROR PROCESSING	01/23/90
5,581,722	MEMORY MANAGEMENT UNIT FOR MANAGING ADDRESS OPERATIONS CORRESPONDING TO DOMAINS USING ENVIRONMENTAL CONTROL	12/03/96
5,613,083	TRANSLATION LOOKASIDE BUFFER THAT IS NON-BLOCKING IN RESPONSE TO A MISS FOR USE WITHIN A MICROPROCESSOR CAPABLE OF PROCESSING SPECULATIVE INSTRUCTIONS	03/18/97
5,442,766	METHOD AND SYSTEM FOR DISTRIBUTED INSTRUCTION ADDRESS TRANSLATION IN A MULTISCALAR DATA PROCESSING SYSTEM	08/15/95
4,954,942	SOFTWARE DEBUGGING SYSTEM FOR WRITING A LOGICAL ADDRESS CONVERSION DATA INTO A TRACE MEMORY OF AN EMULATOR	09/04/90
5,465,337	METHOD AND APPARATUS FOR MEMORY MANAGEMENT UNIT SUPPORTING MULTIPLE PAGES SIZES	11/07/95

5,526,510	METHOD AND APPARATUS FOR IMPLEMENTING A SINGLE CLOCK CYCLE LINE REPLACEMENT IN A DATA CACHE UNIT	06/11/96
5,142,672	DATA TRANSFER CONTROLLER INCORPORATING DIRECT MEMORY ACCESS CHANNELS AND ADDRESS MAPPED INOUT/ OUTPUT WINDOWS	08/25/92
5,561,814	METHODS AND APPARATUS FOR DETERMINING MEMROY OPERATING CHARACTERISTICS FOR GIVEN MEMORY LOCATIONS VIA ASSIGNED ADDRESS RANGES	10/01/96
5,930,832	APPARATUS TO GUARANTEE TLB INCLUSION FOR STOTE OPERATIONS	07/27/99
5,958,061	HOST MICROPROCESSOR WITH APPARATUS FOR TEMPORARILY HOLDING TARGET PROCESSOR STATE	09/28/99
5,805,490	ASSOCIATE MEMORY CIRCUIT AND TLB CIRCUIT	09/08/98
5,282,274	TRANSLATION OF MULTIPLE VIRTUAL PAGES UPON A TLB MISS	01/25/94
4,481,573	SHARED VIRTUAL ADDRESS TRANSLATION UNIT FOR A MULTIPROCESSOR SYSTEMS	11/06/84
5,361,340	APPARATUS FOR MAINTAINING CONSISTENCY IN A MICROPROCESSOR COMPUTER SYSTEM USING VIRTUAL CACHING	11/01/94
4,825,412	LOCKPUT REGISTERS	04/25/89
4,914,577	DYNAMIC MEMORY MANGEMENT SYSTEM AND METHOD	04/03/90
5,577,231	STORAGE ACCESS AUTHORIZATION CONTROLS IN A COMPUTER SYSTEM USING DYNAMIC TRANSLATION OF LARGE ADDRESSES	11/19/96
5,097,409	MULTI-PROCESSOR SYSTEM WITH CACHE MEMORIES	03/17/92
5,623,628	COMPUTER SYSTEM AND METHOD FOR MAINTAINING MEMORY CONSISTENCY IN A PIELINED NON-BLOCKING CACHING BUS REQUEST QUEUE	04/22/97
4,928,225	COHERENT CACHE STRUCTURES AND METHODS	05/22/90
5,197,144	DATA PROCESSOR FOR RELOADING DEFERRED PUSHES IN A COPY-BACK DATA CACHE	03/23/93
5,247,648	MAINTAINING DATA COHERENCY BETWEEN A CENTRAL CACHE, AN I/O CACHE AND A MEMORY	09/21/93
5,317,720	PROCESSOR SYSTEM WITH WRITEBACK CACHE USING WRITEBACK AND NONWRITEBACK TRANSACTIONS STORED IN SEPARATE QUEUES	05/31/94
5,239,646	DATA TRANSMISSION METHOD AND DATA PROCESSING SYSTEM USING THE SAME	08/24/93
4,598,402	SYSTEM FOR TREATMENT OF SINGLE BIT ERROR IN BUFFER STORAGE UNIT	07/01/86
4,458,316	QUEUING COMMANDS IN A PERIPHERAL DATA STORAGE SYSTEM	07/03/84
5,463,767	DATA TRANSFER CONTROL UNIT WITH MEMEORY UNIT FAULT DETECTION CAPABILITY	10/31/95
4,607,331	METHOD AND APPARATUS FOR IMPLEMENTING AN ALGORITHM ASSOCIATED WITH STORED INFORMATION	08/19/86
4,467,411	SCHEDULING DEVICE OPERATIONS IN A BUFFERED PERIPHERAL SUBSYSTEM	08/21/84
3,863,228	APPARATUS FOR DETECTING AND ELIMINATING A TRANSFER OF NOISE RECORDS TO A DATA PROCESSING APPARATUS	01/28/75
5,517,615	MULTICHANNEL INTEGRITY CHECKING DATA TRANSFER SYSTEM FOR CONTROLLING DIFFERENT SIZE DATA BLOCK TRANSFER WITH ON-THE-FLY CHECKOUT OF EACH WORD AND DATA BLOCK TRANSFERRED	05/14/96
5,564,111	METHOD AND APPARATUS FOR IMPLEMENTING A NONBLOCKING TRANSLATION LOOKASIDE BUFFER	10/08/96
5,566,298	METHOD FOR STATE RECOVERY DURING ASSIST AND RESTART IN A DECODER HAVING AN ALIAS MECHANISM	10/15/96
5,574,927	RISC ARCHITECTURE COMPUTER CONFIGURED FOR EMULATION OF THE INSTRUCTION SET OF A TARGET COMPUTER	11/12/96
5,721,927	METHOD FOR VERIFYING CONTIQUITY OF A BINARY TRANSLATED BLOCK OF INSTRUCTIONS BY ATTACHING A COMPARE AND/OR BRANCH INSTRUCTION TO A PREDECESSOR BLOCK OF INSTRUCTIONS	02/24/98
5,768,567	OPTIMIZING HARDWARE AND SOFTWARE CO-SIMULATOR	06/16/98

5,838,948	SYSTEM AND METHOD FOR SIMLUATION OF COMPUTER SYSTEMS COMBINING HARDWARE AND SOFTWARE INTERACTION	11/17/98
5,481,685	RISC MICROPROCESSOR ARCHITECTURE IMPLEMENTING FAST TRAP AND EXCEPTION STATE	01/02/96
5,644,742	PROCESSOR STRUCTURE AND METHOD FORA TIME-OUT CHECKPOINT	07/01/97
5,638,525	PROCESSOR CAPABLE OF EXECUTING PROGRAMS THAT CONTAIN RISC AND CISC INSTRUCTIONS	06/10/97
5,613,090	COMPUTER SYSTEM FOR DISPARATE WINDOWING ENVIRONMENTS WHICH TRANSLATES REQUESTS AND REPLIES BETWEEN THE DISPARATE ENVIRONMENTS	03/18/97
5,604,753	METHOD AND APPARATUS FOR PERFORMING ERROR CORRECTION ON DATA FROM AN EXTERNAL MEMORY	02/18/97
5,598,560	TRACKING CONDITION CODES IN TRANSLATION CODE FOR DIFFERENT MACHINE ARCHITECTURES	01/28/97
5,598,546	DUAL-ARCHITECTURE SUPER-SCALAR PIPELINE	01/28/97
5,574,922	PROCESSOR WITH SEQUENCES OF PROCESSOR INSTRUCTIONS FOR LOCKED MEMORY UPDATES	11/12/96
5,546,552	METHOD FOR TRANSLATING NON-NATIVE INSTRUCTIONS TO NATIVE NSTRUCTIONS AND COMBINING THEM INTO A FINAL BUCKEDT FOR PROCESSING ON A HOST PROCESSOR	08/13/96
5,528,755	INVALID DATA DETECTION RECORDING AND NULLIFICATION	06/18/96
5,507,030	SUCCESSIVE TRANSLATION, EXECUTION AND INTERPRETATION OF COMPUTER PROGRAM HAVING CODE AT UNKNOWN LOCATIONS DUE TO EXECUTION TRANSFER INSTRUCTIONS HAVING COMPUTED DESTINATION ADDRESSES	04/09/96
5,247,628	PARALLEL PROCESSOR INSTRUCTION DISPATCH APPARATUS WITH INTERRUPT HANDLER	09/21/93
4,992,934	REDUCED INSTRUCTION SET COMPUTING APPARATUS AND METHODS	02/12/91

Foreign Patent or Published Foreign Patent Application

Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
					Yes	No
0651331A1	03.05.95	EUROPE	G06F	12/08	X	

The Examiner's attention is respectfully directed to the following related documents:

Halfhill; "EMULATION: RISC'S SECRET WEAPON"; Special Report: The RISC Decision; BYTE April 1994

Andrews et al.; " MIGRATING A CISC COMPUTER FAMILY ONTO RISC VIA OBJECT CODE TRANSLATION"; Tandem Computers, Cupertino, CA 1992 Pgs 213-222; Association of Computing Machinery 1992

Cmelik et al.; "SHADE: A FAST INSTRUCTIONSET SIMULATOR FOR EXECUTION PROFILING"; Association for Computing Machinery 1994

Bedichek;"TALISMAN FAST AND ACCURATE MULTICOMPUTER SIMULATION"; Lab for Computer Science Cambridge MA; Association of Computing Machinery 1995

Ando et al.; "UNCONSTRAINED SPECULATIVE EXECUTION WITH PREDICATED STATE BUFFERING"; System LSI Laboratory, Japan; pgs 126-137; Association of Computing Machinery 1995

May; "MIMIC: A FAST SYSTEM/370 SIMULATOR; IBM Thomas J. Watson Research Center NY; Association of Computing Machinery 1987

Tremblay et al.; "A FAST AND FLEXIBLE PERFORMANCE SIMULATOR FOR MICRO-ARCHITECTURE TRADE-OFF ANALYSIS ON ULTRASPARC-I"; 32nd Design Automation Conference; San Francisco, CA 1995

Kumar et al.; "EMULATION VERIFICATION OF THE MOTOROLA 68060"; Motorola Inc.; Austin, TX; 1995 IEEE

Note et al.; 'RAPID PROTOTYPING OF DSP SYSTEMS: REQUIREMENTS AND SOLUTIONS"; Philips ITCL Belgium; 1995 IEEE

Witchel et al.; " EMBRA FAST AND FLEXIBLE MACHINE SIMULATION"; Sigmetrics ACM 1996; pages 68-79

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Matthew J. Blecher
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Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,349,658	09/20/94	O'Rourke et al.	395	700	11/01/91
	B	5,467,473	11/14/95	Kahle et al.	395	800	01/08/93
	C	5,875,340	02/23/99	Quarnstrom et al.	395	733	05/31/96
	D	5,274,815	12/28/93	Trissel et al.	395	700	11/01/91
	E	6,031,992	02/29/00	Cmelik et al.	395	705	07/05/96
	F	4,530,050	07/16/85	Fukunaga et al.	364	200	08/17/82
	G	5,553,255	09/03/96	Jain et al.	395	375	04/27/95
	H	4,896,257	01/23/90	Ikeda et al.	364	200	11/28/88
	I	5,581,722	12/03/96	Welland	395	417	09/26/94
	J	5,613,083	03/18/97	Glew et al.	395	417	09/30/94
	K	5,442,766	08/15/95	Chu et al.	395	414	10/09/92
	L	4,954,942	09/04/90	Masuda et al.	364	200	11/17/88
	M	5,465,337	11/07/95	Kong et al.	395	417	10/05/94
	N	5,526,510	06/11/96	Akkary et al.	395	460	09/30/94
	O	5,142,672	08/25/92	Johnson et al.	395	500	12/15/87
	P	5,561,814	10/01/96	Glew et al.	395	833	12/22/93
	Q	5,930,832	07/27/99	Heaslip et al.	711	207	06/07/96
	R	5,958,061	09/28/99	Kelly et al.	714	1	07/24/96
	S	5,805,490	09/08/98	Machida	364	784.01	07/10/95
	T	5,282,274	01/25/94	Liu	395	400	05/24/90
	U	4,481,573	11/06/84	Fukunaga et al.	364	200	11/13/81
	V	5,361,340	11/01/94	Kelly et al.	395	400	03/09/93
	W	4,825,412	04/25/89	Sager et al.	365	49	04/01/88
	X	4,914,577	04/03/90	Stewart et al.	364	200	07/16/87
	Y	5,577,231	11/19/96	Scalzi et al.	395	500	12/06/94
	Z	5,097,409	03/17/92	Schwartz et al.	395	425	06/18/91
	AA	5,623,628	04/22/97	Brayton et al.	395	468	03/02/94
	BB	4,928,225	05/22/90	McCarthy et al.	364	200	09/02/88
	CC	5,197,144	03/23/93	Edenfield et al.	395	425	02/26/90
	DD	5,247,648	09/21/93	Watkins et al.	395	425	04/30/92
	EE	5,317,720	05/31/94	Stamm et al.	395	425	03/22/93
	FF	5,239,646	08/24/93	Kimura	395	575	07/02/90
	GG	4,598,402	07/01/86	Matsumoto et al.	371	38	11/07/83
	HH	4,458,316	07/03/84	Fry et al.	364	200	10/11/83
	II	5,463,767	10/31/95	Joichi et al.	395	183.13	02/24/93

U.S. Pat nt Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	JJ	4,607,331	08/19/86	Goodrich, Jr. et al.	364	200	05/13/83
	KK	4,467,411	08/21/84	Fry et al.	364	200	03/06/81
	LL	3,863,228	01/28/75	Taylor	340	172.5	12/13/73
	MM	5,517,615	05/14/96	Sefidvash et al.	395	182.03	08/15/94
	NN	5,564,111	10/08/96	Glew et al.	395	185.06	09/30/94
	OO	5,566,298	10/15/96	Boggs et al.	395	182.08	03/01/94
	PP	5,574,927	11/12/96	Scantlin	395	800	03/25/94
	QQ	5,721,927	02/24/98	Baraz et al.	395	705	08/07/96
	RR	5,768,567	06/16/98	Klein et al.	395	500	05/14/96
	SS	5,838,948	11/17/98	Bunza	395	500	12/01/95
	TT	5,481,685	01/02/96	Nguyen et al.	395	375	11/21/94
	UU	5,644,742	07/01/97	Shen et al.	395	591	06/07/95
	VV	5,638,525	06/10/97	Hammond et al.	395	385	10/02/95
	WW	5,613,090	03/18/97	Willems	395	500	10/05/93
	XX	5,604,753	02/18/97	Bauer et al.	371	40.1	01/04/94
	YY	5,598,560	01/28/97	Benson	395	707	03/07/91
	ZZ	5,598,546	01/28/97	Blomgren	395	385	08/31/94
	AAA	5,574,922	11/12/96	James	395	561	06/17/94
	BBB	5,546,552	08/13/96	Coon et al.	395	375	05/12/95
	CCC	5,528,755	06/18/96	Beardsley et al.	395	185.01	12/22/92
	DDD	5,564,104	10/08/96	Yamashita et al.	395	182.15	08/25/94
	EEE	5,507,030	04/09/96	Sites	395	800	03/07/91
	FFF	5,247,628	09/21/93	Grohoski	395	375	01/17/90
	GGG	4,992,934	02/12/91	Portanova et al.	364	200	03/30/90

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	HHH	0651331A1	03.05.95	EUROPE	G06F	12/08	X	

Other D cum nts

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	III	Halfhill; "EMULATION: RISC'S SECRET WEAPON"; Special Report: The RISC Decision; BYTE April 1994
	JJJ	Andrews et al.; " MIGRATING A CISC COMPUTER FAMILY ONTO RISC VIA OBJECT CODE TRANSLATION" ; Tandem Computers, Cupertino, CA 1992 Pgs 213-222; Association of Computing Machinery 1992
	KKK	Cmelik et al.; "SHADE: A FAST INSTRUCTIONSET SIMULATOR FOR EXECUTION PROFILING"; Association for Computing Machinery 1994
	LLL	Bedichek ;"TALISMAN FAST AND ACCURATE MULTICOMPUTER SIMULATION"; Lab for Computer Science Cambridge MA; Association of Computing Machinery 1995
	MMM	Ando et al.; "UNCONSTRAINED SPECULATIVE EXECUTION WITH PREDICATED STATE BUFFERING"; System LSI Laboratory, Japan ; pgs 126-13; Association of Computing Machinery 1995
	NNN	May; "MIMIC: A FAST SYSTEM/370 SIMULATOR; IBM Thomas J. Watson Research Center NY; Association of Computing Machinery 1987
	OOO	Tremblay et al.; "A FAST AND FLEXIBLE PERFORMANCE SIMULATOR FOR MICRO-ARCHITECTURE TRADE-OFF ANALYSIS ON ULTRASPARC-I"; 32nd Design Automation Conference; San Francisco, CA 1995
	PPP	Kumar et al.; "EMULATION VERIFICATION OF THE MOTOROLA 68060"; Motorola Inc.; Austin, TX; 1995 IEEE
	QQQ	Note et al.; 'RAPID PROTOTYPING OF DSP SYSTEMS: REQUIREMENTS AND SOLUTIONS"; Philips ITCL Belgium; 1995 IEEE
	RRR	Witchel et al.; " EMBRA FAST AND FLEXIBLE MACHINE SIMULATION"; Sigmetrics ACM 1996; pages 68-79

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.